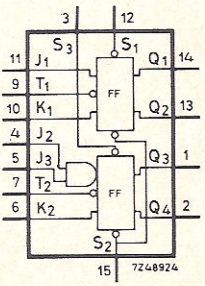
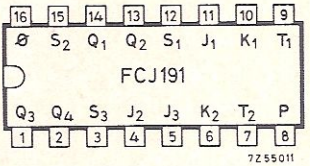
The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

development sample data

DUAL JK MASTER-SLAVE FLIP-FLOP





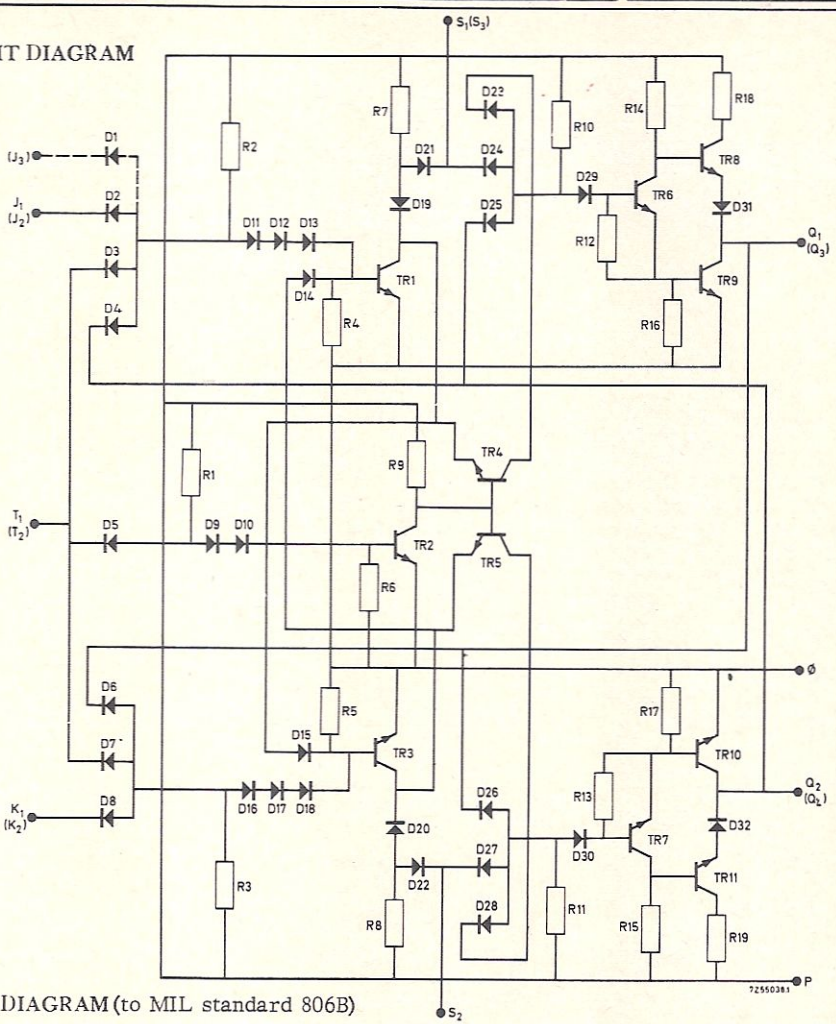
Package XG14; dual in-line

QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Clock rate	f_c	typ. 7	MHz
Available d.c. fan-out T_{amb} = 0 to +75 °C	N_a	⩾ 8	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 100	mW

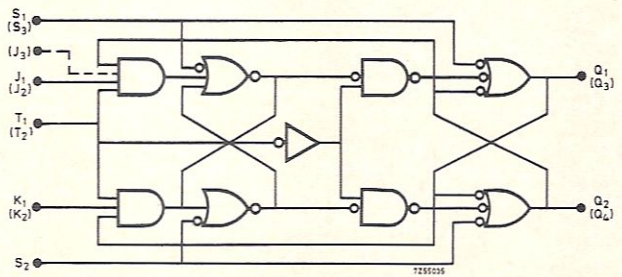
The FCJ191 comprises two independent direct coupled JK flip-flops, operating on the master-slave principle. Operating depends on voltage levels only, e.g. rise and fall times of all inputssignals including the trigger signal are immaterial. The set and reset inputs (overriding any other inputs) are active at the LOW level. Typical applications include counters and shift registers.

These data, based on the specifications and measured performance of development samples, afford a preliminary indication of the characteristics to be expected of the described product. Distribution of development samples implies no guarantee as to the subsequent availability of the product

CIRCUIT DIAGRAM



LOGIC DIAGRAM (to MIL standard 806B)



FUNCTION TABLES

1. Trigger action via T terminal (each flip-flop)

T = HIGH		T = LOW	
J_1 J	K_1 K_2	Q_1 Q_3	Q_2 Q_4
H	H	reversed	
L	H	L	H
H	L	H	L
L	L	no change	

The information on J and K is transferred into the master by T going HIGH. When T subsequently goes LOW the outputs will assume the levels shown in the table.
Inputs S_1, S_2 and S_3 should be HIGH or floating.

For the flip-flop with two J-inputs is $J = J_2 \cdot J_3$ for positive logic

2. Set or reset via S terminals

S_1 S_3	S_2 S_2	Q_1 Q_3	Q_2 Q_4
H	L	L	H
L	H	H	L
L	L	H	H
H	H	no change	

The set inputs override the other inputs and directly determine the outputs of the relevant flip-flop.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS (Limiting values) [1]

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_J, V_K, V_T, V_S	max.	8.0	V
Output current [2]	$-I_Q$	max.	20	V
Input current [3]	$-I_J, -I_K, -I_T, -I_S$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}	−55 to +125		°C
Operating ambient temperature	T_{amb}	0 to +75		°C

1) Limiting values according to the Absolute Maximum System as defined in IEC publication 134.
2) For negative output voltage in LOW state.
3) At this limit input voltage typ. : −1.5 V

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +75	°C
Uniform system supply voltage	V_P		5.7 to 6.3	V
Available d.c. fan out				
to T input	N_{aT}	⩾	3	
to J or K input	$N_{aJ} = N_{aK}$	⩾	10	
to S input	N_{aS2}	⩾	2	
	$N_{aS1} = N_{aS3}$	⩾	4	
to G input	N_{aG}	⩾	8	
D.C. noise margin				
to T input	M_L	min.	0.3	V
	M_H	min.	1.3	V
to J or K input	M_L	min.	0.7	V
	M_H	min.	1.3	V
to S input	M_L	min.	0.3	V
	M_H	min.	2.0	V
to G input	M_L	min.	0.4	V
	M_H	min.	1.6	V
Average propagation delay time	t_{pd}	max.	105	ns
Maximum clock rate	f_c	⩾	5	MHz
Equivalent input capacitances				
for T input	C_T	typ.	12	pF
for J or K input	$C_J = C_K$	typ.	4	pF
for S input	C_{S2}	typ.	16	pF
	$C_{S1} = C_{S3}$	typ.	8	pF
Supply current (duty cycle 50%) [1]	I_{Pav}	typ.	16.8	mA
Power dissipation at T_{amb} = 75 °C [1]	P_{tot}	max.	150	mW

[1]) Both flip-flops together

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	+25	+75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	14.0 16.0	16.5 19.0	12.4 14.4	mA mA	5.7 6.3	
Output voltage HIGH	V_{QHmin}	3.9	4.0	4.1	V	5.7	$I_Q = -100\ \mu A$
Output voltage HIGH (lowest permissible) at: Output current HIGH	V_{QHPmin} $-I_{QHmax}$	3.6 0.85	3.3 3.3	3.0 5.5	V mA	5.7 5.7	
Input current LOW	$-I_{JLmax}$, $-I_{KLmax}$	1.4 1.6	1.3 1.5	1.2 1.4	mA mA	5.7 6.3	$V_J = V_K = 0.4$ V; other inputs floating
	$-I_{TLmax}$	4.0 4.5	3.8 4.2	3.5 3.9	mA mA	5.7 6.3	$V_T = 0.4$ V; other inputs floating
	$-I_{S2Lmax}$	5.7 6.6	5.5 6.3	5.2 5.8	mA mA	5.7 6.3	$V_S = 0.4$ V; other inputs floating
	$-I_{S1Lmax}$ $-I_{S3Lmax}$	2.9 3.3	2.8 3.2	2.6 2.9	mA mA	5.7 6.3	$V_S = 0.4$ V; other inputs floating
Input current HIGH	I_{JHmax}, I_{KHmax}	1	1	25	μA	5.7	$V_J = V_K = 5.3$ V other inputs 0 V
	I_{THmax}	3	3	75	μA	5.7	$V_T = 5.3$ V other inputs 0 V
	I_{S2Hmax}	4	4	100	μA	5.7	$V_S = 5.3$ V other inputs 0 V
	I_{S1Hmax} I_{S3Hmax}	2	2	50	μA	5.7	$V_S = 5.3$ V other inputs 0 V
Supply current (both flip-flops together)	I_{Pmax}	-	26.7	-	mA	6.3	T input LOW J, K, S inputs HIGH

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references		
		0	+25	+75		V_P (V)		fig.
DYNAMIC DATA						5.7 and 6.3		
Change of state								
Input voltage HIGH during:	V_{THmin} V_{JHmin} V_{KHmin}	2.6	2.3	1.9	V		HIGH level at T and J and/or K to be present simultaneously	1
Input time HIGH to:	t_{THmin}	60	60	60	ns			1
T-input voltage LOW	V_{TLmax}	1.0	1.0	0.7	V		$t_{TLmin} = t_{pdf}$	1
No change of state								
J/K input voltage LOW	V_{JLmax} V_{KLmax}	1.6	1.4	1.1	V		LOW level at J and K to be present prior to T turning HIGH and to remain present during T is HIGH	2
Clock skew protection								
Hold time	$t_{hold\,max}$	10	10	10	ns			2
Reset								
S input voltage LOW	V_{SLmax}	1.0	1.0	0.7	V		active $t_{SLmin} = t_{pdf}$	3
S input voltage HIGH	V_{SHmin}	1.9	1.8	1.6	V		inactive	
DYNAMIC DATA								
Propagation delay times from T to Q								
Rise propagation delay time	$t_{pdr\,max}$	–	90	–	ns	6.0	$V_{pd} = 1.5$ V N = 1; $C_w = 60$ pF	4
Fall propagation delay time	$t_{pdf\,max}$	–	120	–	ns	6.0	$V_{pd} = 1.5$ N = 8; $C_w = 30$ pF other output: N = 1; $C_w = 60$ pF	4

CHARACTERISTICS (continued)

DYNAMIC DATA

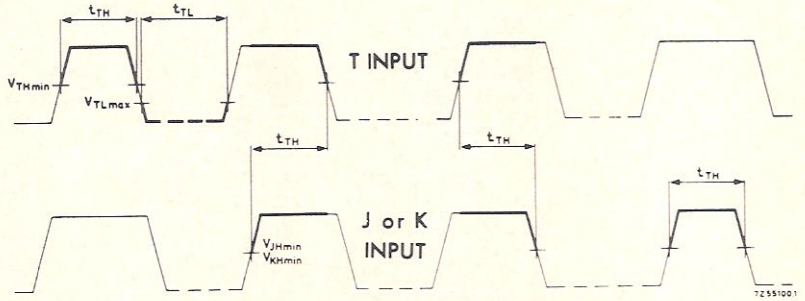


Fig. 1. Waveforms illustrating conditions for change of state.

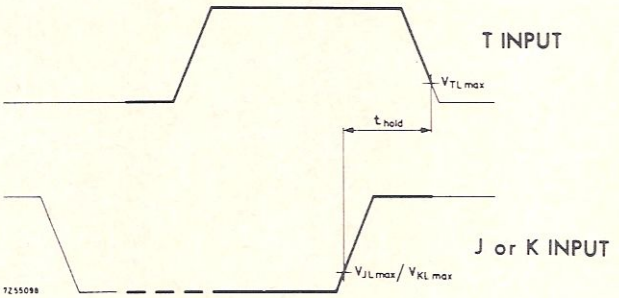


Fig. 2. Waveforms illustrating conditions for no change of state.

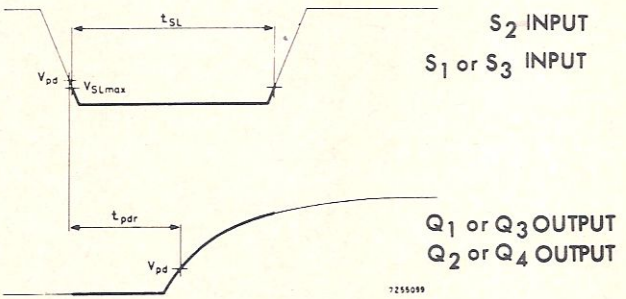
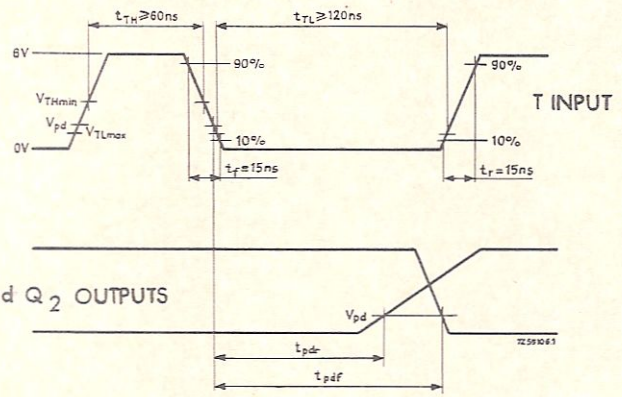
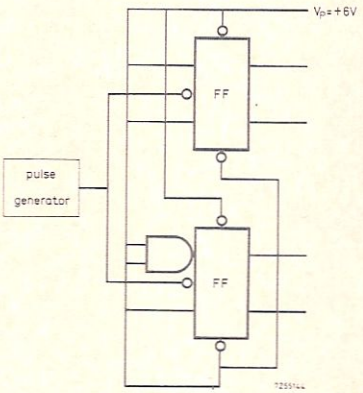


Fig. 3. Waveforms illustrating conditions for set or reset.

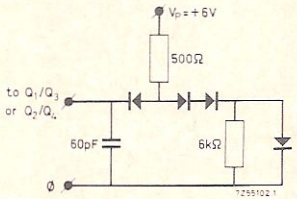
CHARACTERISTICS (continued)

DYNAMIC DATA

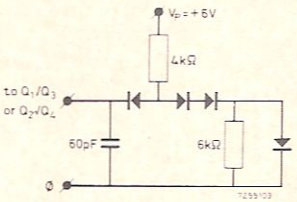




$C_L = C_W + C_i(N - 1)$



Diodes FCY101
Equivalent load for N = 8 and C_W = 30 pF



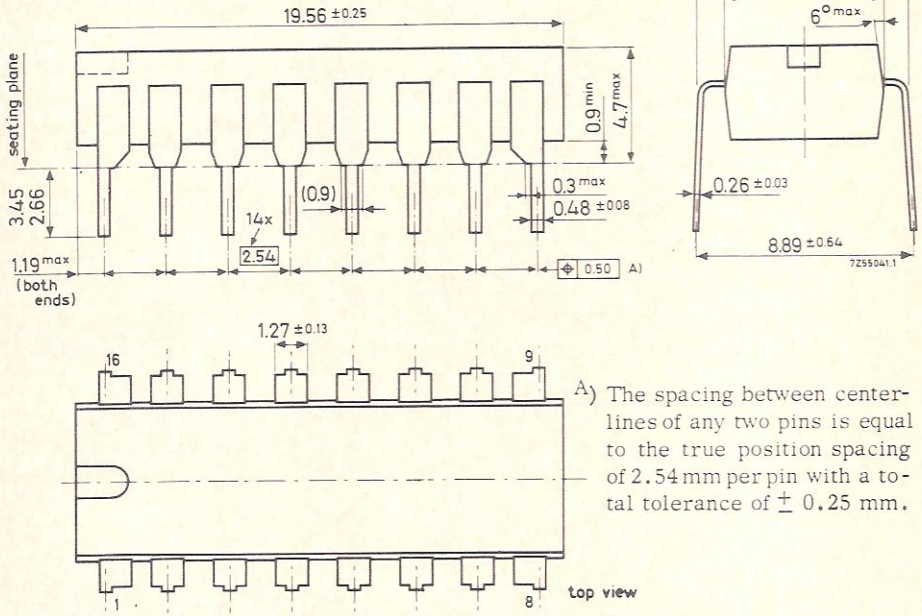
Diodes FCY101
Equivalent load for N = 1 and C_W = 60 pF

Fig. 4. Waveforms and loading circuits illustrating measurement of t_{pdr} and t_{pdf}.

PACKAGE OUTLINE

XG14; dual in-line

Dimensions in mm



A) The spacing between centerlines of any two pins is equal to the true position spacing of 2.54 mm per pin with a total tolerance of ± 0.25 mm.

Handling notes

1. Devices may be soldered directly into circuits with soldering irons. At iron temperatures below 245 °C the maximum soldering time should be less than 10 seconds and at iron temperatures between 245 °C and 400 °C the soldering time should be less than 5 seconds. In both cases the soldering iron should be applied below the seating plane (see outline drawing).
2. Devices mounted up to the seating plane on a printed circuit board may be dip or flow soldered providing the solder temperature is below 245 °C and the time of immersion is less than 5 seconds. The body temperature should not be allowed to exceed the maximum storage temperature during soldering. If excessive preheat cycles are used, it may be necessary to cool the printed board immediately after leaving the solder bath/wave in order that this requirement is met.